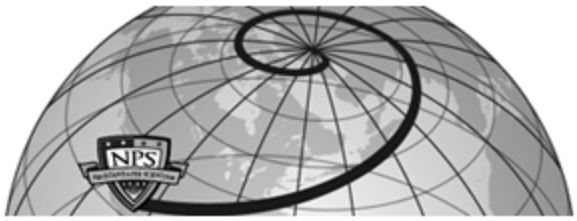

AC BIAS FOR A MAGNETIC AMPLIFIER

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by

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Lieutenant Commander, United States Navy

Submitted in partial fulfillment of
the requirements for the degree of

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IN

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ABSTRACT

The use of an alternating bias for a center tap doublet circuit, as a typical representative of the doublet class of magnetic amplifiers, was investigated primarily to determine if a lower minimum output could be obtained than with a direct bias without appreciably changing the gain characteristic. An analytical solution to the problem indicated that a minimum output less than that obtainable with a DC bias alone could be obtained without a major change in the gain characteristic. Laboratory investigation revealed that a minimum output was obtainable that was significantly less than that obtainable by use of a DC bias alone by using an AC bias in conjunction with a DC bias.

The writer wishes to express his appreciation to Mr. Raymond B. Yarbrough of the U. S. Naval Postgraduate School whose inspiration and assistance made this investigation possible.

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1. Introduction

Magnetic amplifiers have enjoyed a resurgence of interest and application in recent years due to the availability of square loop magnetic materials and high quality solid state diodes. The so called "doublet class" of magnetic amplifiers has found wide spread usage as a class of single ended D. C. amplifiers. One disadvantage of this class of amplifiers, when not used in a push pull configuration, has been a minimum output above zero with no control signal. For a DC biased amplifier a minimum of 150% of the magnetizing current for the core employed is ordinarily realized.

This investigation was concerned with the reduction of this minimum by the use of an AC powered bias winding. As a representative circuit of the "doublet class" the "center tap" circuit was analyzed and tested in the laboratory. In the analysis of the circuit the method developed by Johannessen was employed.[1]

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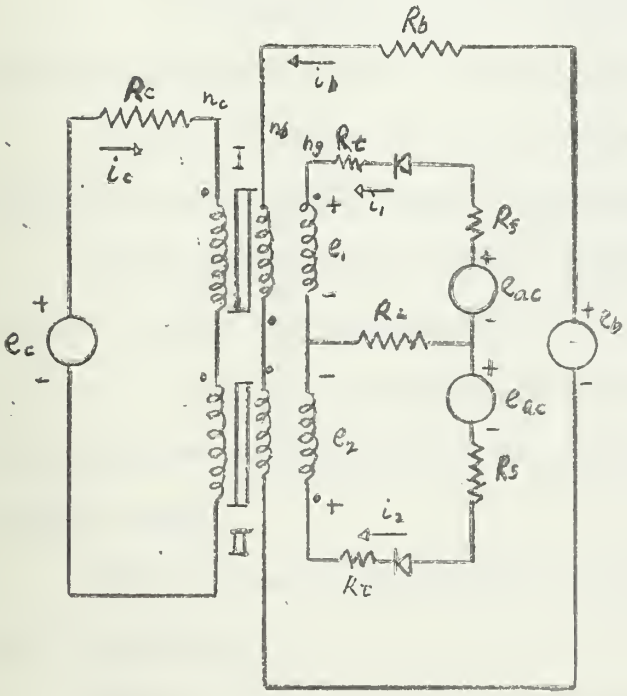
[1] P. R. Johannessen, "Analysis of Magnetic Amplifiers by the use of Difference Equations", AIEE Transactions, Vol. 70 part 1, pp 700-711, January 1955.

2. Analysis of Circuit

The circuit chosen for analysis was the center tap doublet circuit, Figure 1, as a representative of the "doublet class" of magnetic amplifiers. The method of analysis was based upon writing a set of linear equations describing the circuit relationships for specified modes of operation. The boundary line between modes of operation was determined by consideration of the fact that after the first cycle the amount of flux change per cycle was zero. Basically this is the consideration that the core reaches saturation only once each cycle.

Figure 1

Center Tap Doublet Magnetic Amplifier



e_c	DC control voltage
R_c	control resistance
n_c	number of control turns
e_b	AC bias voltage
R_b	AC bias resistance
n_b	number of turns of ac bias winding
e_{ac}	AC supply voltage
R_s	Ac supply resistance
R_f	Diode forward resistance
R_t	Winding resistance
R_l	Load resistance
n_g	number of turns of source or gating winding

The following assumptions were made in the analysis and were later checked for validity:

1. e_c is constant or so slowly varying in comparison with e_{ac} that it can be approximated by its average value over one half-cycle.

2. The cores and diodes are matched.

3. The core can be modeled by a square resistive model, with static width F_o, and with the width increasing linearly with the rate of change of flux. $F = \pm F_o + K \frac{d\phi}{dt}$. Referred to the gating circuit this becomes $\Sigma i = \pm I_o + G e$. The sign associated with I_o is determined by the sign of e.

4. The diode in the forward direction has resistance R_f with a forward voltage drop V_f and in the reverse direction an infinite resistance.

5. The diode does not unblock in the resetting half-cycle nor block in the gating half-cycle.

Diode Blocking is here defined as the reverse biasing of the diode associated with the gating core.

Diode Unblocking is here defined as the forward biasing of the diode associated with the resetting core.

6. That e_{ac} is adjusted to take the core from positive to negative saturation in one half-cycle in the absence of any other signal.

With these assumptions the following modes of operation are obtained:

Mode A (both cores unsaturated, core I gating, core II

resetting),

Mode B (core I saturated, core II resetting),

Mode C (both cores unsaturated, core I resetting, core II gating),

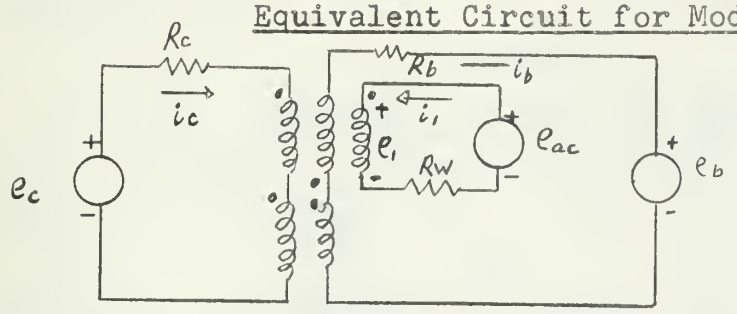
Mode D (core I resetting, core II saturated).

The term "gating" refers to change of flux along the hysteresis loop under the influence of the source voltage and occurs when the diode is unblocked in the positive half-cycle of the source voltage. Resetting is the change of flux along the hysteresis loop in the opposite direction. Due to the symmetry of the circuit operation, mode C equations are the same as mode A equations except for the sign of the source and bias voltage. Operation in mode D is likewise analogous to operation in mode B.

Mode A. Both cores unsaturated, core I gating, core II resetting.

Figure 2

Equivalent Circuit for Mode A



$$R_w = R_t + R_f + R_s + R_L$$

$$N = \frac{n_g}{n_c} \qquad N_b = \frac{n_g}{n_b}$$

Equations for Mode A operation.

$$e_c = i_c R_c + \frac{e_2}{N} + \frac{e_1}{N}$$

$$e_{ac} - V_f = i_1 R_w + e_1$$

$$e_b = i_b R_b + \frac{e_2}{N_b} - \frac{e_1}{N_b}$$

$$\frac{i_c}{N} - \frac{i_b}{N_b} + i_1 = I_o + G e_1$$

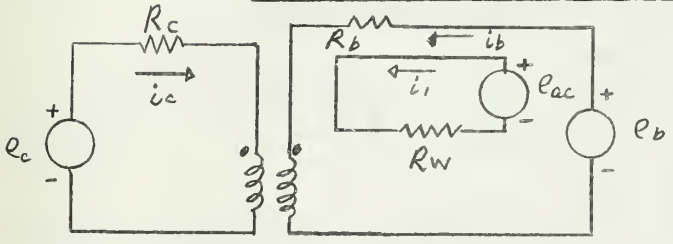
$$\frac{i_c}{N} + \frac{i_b}{N_b} = -I_o + G e_2$$

$$\begin{pmatrix} e_c \\ e_{ac}-V_F \\ e_b \\ I_o \\ I_o \end{pmatrix} = \begin{pmatrix} R_c & 0 & 0 & \frac{1}{N} & \frac{1}{N} \\ 0 & R_w & 0 & 1 & 0 \\ 0 & 0 & R_b & -\frac{1}{N_b} & \frac{1}{N_b} \\ \frac{1}{N} & 1 & -\frac{1}{N_b} & -G & 0 \\ -\frac{1}{N} & 0 & -\frac{1}{N_b} & 0 & G \end{pmatrix} \begin{pmatrix} i_c \\ i_1 \\ i_b \\ e_1 \\ e_2 \end{pmatrix}$$

Mode B. Core I saturated. Core II resetting.

Figure 3

Equivalent Circuit for Mode B



Equations for Mode B operation.

$$e_c = i_c R_c + \frac{e_2}{N}$$

$$e_{ac} - V_F = i_1 R_w$$

$$e_b = i_b R_b + \frac{e_2}{N_b}$$

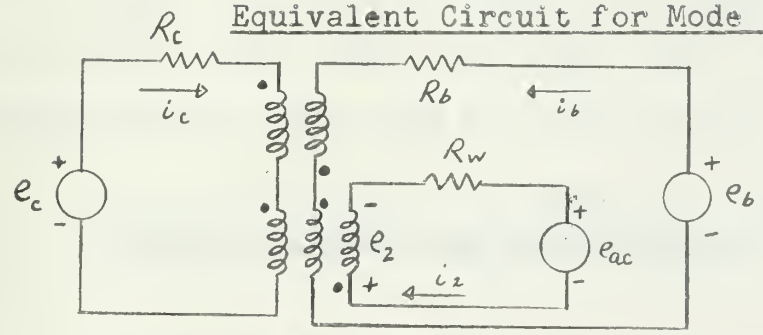
$$\frac{i_c}{N} + \frac{i_b}{N_b} = -I_o + G e_2$$

$$\begin{pmatrix} e_c \\ e_{ac}-V_F \\ e_b \\ I_o \end{pmatrix} = \begin{pmatrix} R_c & 0 & 0 & \frac{1}{N} \\ 0 & R_w & 0 & 0 \\ 0 & 0 & R_b & \frac{1}{N_b} \\ -\frac{1}{N} & 0 & -\frac{1}{N_b} & G \end{pmatrix} \begin{pmatrix} i_c \\ i_1 \\ i_b \\ e_2 \end{pmatrix}$$

Mode C. Both cores unsaturated, core I resetting, core II gating. This is the dual of Mode A with core I interchanged with core II.

Figure 4

Equivalent Circuit for Mode C



Equations for Mode C operation.

$$e_c = i_c R_c + e_1/N + e_2/N$$

$$-e_{ac} - V_F = i_2 R_w + e_2$$

$$e_b = i_b R_b - e_1/N_b + e_2/N_b$$

$$i_c/N - i_b/N_b = -I_0 + G e_1$$

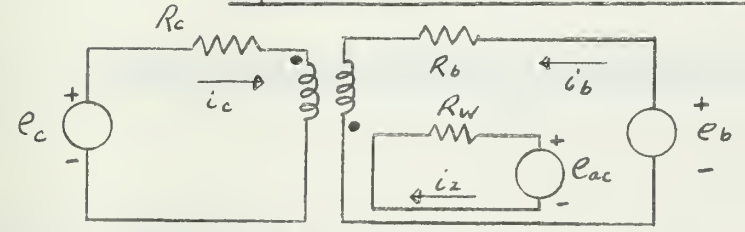
$$i_2 + i_c/N + i_b/N_b = I_0 + G e_2$$

$$\begin{pmatrix} e_c \\ e_{ac}+V_F \\ e_b \\ I_0 \\ I_0 \end{pmatrix} = \begin{pmatrix} R_c & 0 & 0 & 1/N & 1/N \\ 0 & -R_w & 0 & 0 & -1 \\ 0 & 0 & R_b & -1/N_b & 1/N_b \\ -1/N & 0 & 1/N_b & G & 0 \\ 1/N & 1 & 1/N_b & 0 & -G \end{pmatrix} \begin{pmatrix} i_c \\ i_2 \\ i_b \\ e_1 \\ e_2 \end{pmatrix}$$

Mode D. Core I resetting, core II gating. This is the dual of Mode B.

Figure 5

Equivalent Circuit for Mode D



Equations for Mode D operation.

$$e_c = i_c R_c + e_1/N$$

$$-e_{ac} - V_F = i_2 R_w$$

$$e_b = i_b R_b - e_1/N_b$$

$$i_c/N - i_b/N_b = -I_0 + G e_1$$

$$\begin{pmatrix} e_c \\ e_{ac}+V_F \\ e_b \\ I_0 \end{pmatrix} = \begin{pmatrix} R_c & 0 & 0 & 1/N \\ 0 & -R_w & 0 & 0 \\ 0 & 0 & R_b & -1/N_b \\ -1/N & 0 & 1/N_b & G \end{pmatrix} \begin{pmatrix} i_c \\ i_2 \\ i_b \\ e_1 \end{pmatrix}$$

For simplification the following abbreviations are adopted; $\frac{1}{R_c N^2} = G_c$, $\frac{1}{R_b N_b^2} = G_b$, $\frac{1}{R_w} = G_w$. The system determinant for Mode A is $-R_b R_c R_w D$, and that for Mode B is $R_b R_c R_w D'$, where $D = G^2 + 2GG_b + 2GG_c + 4G_c G_b + GG_w + G_b G_w + G_c G_w$ and $D' = G + G_c + G_b$. Solving for e_{1A} (e_1 in mode A), e_{1C}, e_{1D}, i_{1A}, i_{1B}, i_{2C}, and i_{2D} yields:

$$e_{1A} = \frac{\frac{e_c}{NR_c}(G+2G_b) + \frac{e_b}{N_b R_b}(-G-2G_c) + I_o(-G-2G_c) + \frac{e_{ac}-V_F}{R_w}(G+G_c+G_b)}{D}$$

$$e_{1C} = \frac{\frac{e_c}{NR_c}(G+2G_b+G_w) + \frac{e_b}{N_b R_b}(-G-2G_c-G_w) + I_o(G+2G_c+G_w) + \frac{e_{ac}+V_F}{R_w}(G_c-G_b)}{D}$$

$$e_{1D} = \frac{\frac{e_c}{NR_c} - \frac{e_b}{N_b R_b} + I_o}{D'}$$

$$i_{1A} = \frac{\frac{e_c}{NR_c}(-G_w(G+2G_b)) + \frac{e_b}{N_b R_b}(G_w(G+2G_c)) + I_o(G_w(G+2G_c)) + \frac{e_{ac}-V_F}{R_w}(G+2G_c)(G+2G_b)}{D}$$

$$i_{1B} = \frac{e_{ac}-V_F}{R_w}$$

$$i_{2C} = \frac{\frac{e_c}{NR_c}(-G_w(G+2G_b)) + \frac{e_b}{N_b R_b}(-G_w(G+2G_c)) + I_o(G_w(G+2G_c)) + \frac{e_{ac}+V_F}{R_w}(-(G+2G_c)(G+2G_b))}{D}$$

$$i_{2D} = \frac{-e_{ac}-V_F}{R_w}$$

Knowing that the net change of flux in each core is zero for a cycle which begins with resetting yields:

$$\int_0^{T_1} e_{1A}\,dt + \int_{\frac{\pi}{\omega}}^{T_2} e_{1C}\,dt + \int_{T_2}^{\frac{2\pi}{\omega}} e_{1D} = 0$$

Where T_1 and T_2 are the times of modal sequence change. Choosing a square wave excitation, $e_{ac} = -E_{ac}(-1)^n$, $e_b = -E_b(-1)^n$, and, $e_c = E_c$, where the n represents the half-cycle in question yields:

$$-\frac{T_1}{D}\left[\frac{E_c(n)}{NR_c}(G+2G_b)+\frac{E_b}{N_bR_b}(-G-2G_c)+I_o(G-2G_c)+\frac{E_{ac}-V_F}{R_w}(G+G_c+G_b)\right]=$$

$$\frac{T_2-\frac{\pi}{\omega}}{D}\left[\frac{E_c(n+1)}{NR_c}(G+2G_b+G_w)+\frac{E_b}{N_bR_b}(G+2G_c+G_w)+I_o(G+2G_c+G_w)+\frac{E_{ac}-V_F}{R_w}(G_b-G_c)\right]+$$

$$\frac{\frac{2\pi}{\omega}-T_2}{D'}\left[\frac{E_c(n+1)}{NR_c}+\frac{E_b}{N_bR_b}+I_o\right]=\frac{T_2-\frac{\pi}{\omega}}{DD'}\left[\frac{E_c(n+1)}{NR_c}(G+2G_b)(G_b-G_c)+\frac{E_b}{N_bR_b}(G+2G_c)(G_c-G_b)+\right.$$

$$\left.I_o(G+2G_c)(G_c-G_b)+\frac{E_{ac}-V_F}{R_w}(G_b-G_c)(G+G_b+G_c)\right]+\frac{\frac{\pi}{\omega}}{D'}\left[\frac{E_c(n+1)}{NR_c}+\frac{E_b}{N_bR_b}+I_o\right]$$

equation (2.1)

Defining the half-cycle average current as I_L yields:

$$I_L(n)=\frac{\omega}{\pi}\left[\int_0^{T_1} i_{1A}\,dt+\int_{T_1}^{\pi} i_{1B}\,d\tau\right]=\frac{\omega}{\pi}\left[\frac{T_1}{D}\left[\frac{E_c(n)}{NR_c}(-G_w(G+2G_b))+\frac{E_b}{N_bR_b}(G_w(G+2G_c))+\right.\right.$$

$$\left.\left.I_o(G_w(G+2G_c))+\frac{E_{ac}-V_F}{R_w}(G+2G_c)(G+2G_b)\right]+\left(\frac{\pi}{\omega}-T_1\right)\left(\frac{E_{ac}-V_F}{R_w}\right)\right]$$

$$I_L(n)-\left(\frac{E_{ac}-V_F}{R_w}\right)=\frac{\omega}{\pi}\left[\frac{T_1}{D}\left[\frac{E_c(n)}{NR_c}(-G_w(G+2G_b))+\frac{E_b}{N_bR_b}(G_w(G+2G_c))+I_o(G_w(G+2G_c))+\right.\right.$$

$$\left.\left.\frac{E_{ac}-V_F}{R_w}(-G_w(G+G_b+G_c))\right]\right]$$

$$I_L(n+1)=\frac{\omega}{\pi}\left[\int_{\frac{\pi}{\omega}}^{T_2} i_{2C}\,dt+\int_{T_2}^{\frac{2\pi}{\omega}} i_{2B}\,dt\right]$$

$$I_L(n+1)-\left(\frac{E_{ac}-V_F}{R_w}\right)=\frac{\omega}{\pi}\left[\frac{T_2-\frac{\pi}{\omega}}{D}\left[\frac{E_c(n+1)}{NR_c}(G_w(-G-2G_b))+\frac{E_b}{N_bR_b}(G_w(G+2G_c))+\right.\right.$$

$$\left.\left.I_o(G_w(G+2G_c))+\frac{E_{ac}-V_F}{R_w}(-G_w(G+G_b+G_c))\right]\right]$$

Substituting values for $I_L(n)$ and $I_L(n+1)$ into the volt-second equation (2.1) yields:

$$\left[I_L(n)-\left(\frac{E_{ac}-V_F}{R_w}\right)\right]\frac{1}{G_w}=\left[I_L(n+1)-\left(\frac{E_{ac}-V_F}{R_w}\right)\right]\left[\frac{G_b-G_c}{-G_w(G+G_b+G_c)}\right]+\frac{1}{G+G_b+G_c}\left[\frac{E_c(n+1)}{NR_c}+\frac{E_b}{N_bR_b}+I_o\right]$$

This yields the following difference equation:

$$(G+G_b+G_c)\,\bar{I}_L(n)+(G_b-G_c)\,\bar{I}_L(n+1)=\frac{E_{ac}-V_F}{R_w}(G+2G_b)+\left(\frac{E_c(n+1)}{NR_c}+\frac{E_b}{N_bR_b}+I_o\right)G_w$$

In steady state $\bar{I}_L(n) = \bar{I}_L(n+1)$, with the assumptions of matched cores and diodes, the following gain equations are obtained:

$$\bar{I}_L=\frac{E_c}{NR_c}\left(\frac{G_w}{G+2G_b}\right)+\frac{E_b}{N_bR_b}\left(\frac{G_w}{G+2G_b}\right)+I_o\left(\frac{G_w}{G+2G_b}\right)+\frac{E_{ac}-V_F}{R_w}$$

$$\bar{I}_L = K E_c + K_1 \quad \text{for steady state where}$$

$$K=\frac{G_w}{NR_c(G+2G_b)}\quad,\quad K_1=\frac{E_b}{N_bR_b}\left(\frac{G_w}{G+2G_b}\right)+I_o\left(\frac{G_w}{G+2G_b}\right)+\frac{E_{ac}-V_F}{R_w}$$

The minimum output must occur when the core does not saturate in either half cycle, gating or resetting. For the modal sequence we have adopted (A B C D) modes B and D would not exist. Hence $\int_0^{\frac{\pi}{\omega}} e_{1A}\,dt+\int_{\frac{\pi}{\omega}}^{\frac{2\pi}{\omega}} e_{1C}\,dt=0$. Substituting values yields at minimum output:

$$\frac{E_c}{NR_c}\left(G_w+2(G+2G_b)\right)+\frac{E_b}{N_bR_b}(G_w)+I_o(G_w)+\frac{E_{ac}-V_F}{R_w}(G+2G_b)=0$$

Setting $E_c=0$ $$\frac{E_b}{N_bR_b}=-I_o-\frac{E_{ac}-V_c}{R_w}\left(\frac{G+2G_b}{G_w}\right)$$

This value of $\frac{E_b}{N_bR_b}$ when substituted in the gain equation gives a value of zero output with no control signal.

It is now necessary to see if this value of $\frac{E_b}{N_bR_b}$ meets the assumptions of no diode unblocking during the reset half-cycle and blocking during the gating half-cycle. No unblocking

will occur in the resetting half cycle if: $e_{1c} + i_{2c}R_L + e_{ac} + V_F > 0$

$$e_{1c} + R_L i_{2c} + e_{ac} + V_f = \frac{1}{D}\left[\frac{E_c}{NR_c}(G+2G_b+G_w) + \frac{E_b}{N_b R_b}(G+2G_c+G_w) + I_o(G+2G_c+G_w) + \right.$$

$$\frac{E_{ac}-V_F}{R_w}(G_b-G_c) + \frac{E_c}{NR_c}\left(\frac{R_L}{R_w}(-G-2G_b)\right) + \frac{E_b}{N_b R_b}\left(\frac{R_L}{R_w}(G+2G_c)\right) + I_o\left(\frac{R_L}{R_w}(G+2G_c)\right) +$$

$$\frac{E_{ac}-V_F}{R_w}(G+2G_c)(G+2G_b)R_L + \frac{E_{ac}+V_F}{R_W}\left[\frac{(G+2G_b)(G+2G_c)}{G_w} + G_b + G_c + G\right]$$

for $E_c = 0$ and $\frac{E_b}{N_b R_b} = -I_o - \frac{E_{ac}-V_F}{R_w}\left(\frac{G+2G_b}{G_w}\right)$

$$e_{1c} + i_{2c}R_L + e_{ac} + V_F = 2V_F > 0$$

This indicates that no unblocking of the resetting core diode will occur in this situation.

Considering now whether the diode in the gating circuit blocks before the minimum output is reached, we substitute the value for $\frac{E_b}{N_b R_b}$ that should produce zero output with no control voltage into the current expression for i_{1_A} to see if the current remains equal to or greater than zero, indicating no blocking. With this substitution:

$$i_{1_A} D = -I_o(G_w(G+2G_c)) - \left(\frac{E_{ac}-V_F}{R_w}\right)(G+2G_c)(G+2G_b) + I_o(G_w(G+2G_c)) + \left(\frac{E_{ac}-V_F}{R_w}\right)(G+2G_c)(G+2G_b) = 0$$

This result indicates no blocking of the diode in the gating circuit should occur with e_b adjusted for minimum output.

The remaining test to be made is to insure that with the AC bias voltage adjusted for the assumed minimum output that the operation is in the mode sequence assumed. A deviation in the assumed modal sequence would arise if the resetting core

saturated in the reset half-cycle. In order to make this test it is convenient to find the amount of flux change in the resetting core, assuming it does not saturate in one half-cycle, and compare it to the flux required to saturate the core. With the AC bias adjusted for assumed minimum output, the flux change in terms of volt-seconds is $\int_0^{\pi} e_{1c}\, d\tau = (E_{ac} - V_F)\pi$. To find the volt-seconds required to saturate the core the source voltage, e_{ac}, is considered to be adjusted to just reach saturation for the core (from negative to positive saturation or vice versa) in one half-cycle. If e_{ac} is adjusted to this value, the total volt-seconds available from the core referred to the gate windings is found to be $\pi\left(\frac{(E_{ac}-V_F) - I_o R_w}{1+GR_w}\right)$ which will always be less than the volt-seconds required by the resetting core if it is not to saturate. Hence a change in modal sequence will always be encountered prior to reaching the assumed minimum.

Another consideration, in attempting to predict a minimum output, is the fact that at minimum output gating voltage equals the resetting voltage, $e_{1a} + e_2 A = 0$. This gives

$$\frac{e_c}{N R_c}\left(G_w + 2(G+2G_b)\right) + \frac{e_b}{N_b R_b}(G_w) + I_o(G_w) + \left(\frac{e_{ac}-V_F}{R_w}\right)(G+2G_b) = 0$$

Considering sinusoidal excitation this is possible only if two bias windings are employed, an AC and a DC. The DC bias voltage must be adjusted such that $e_c = -\frac{I_o(G_w) N R_c}{G_w + 2(G+2G_b)}$ and the AC bias voltage adjusted such that

$$e_b = -(e_{ac} - V_F)(G+2G_b) R_b N_b \quad \text{as } G_b = \frac{1}{N_b^2 R_b}, \quad e_b = -(e_{ac}-V_F)\left(G N_b R_b + \frac{2}{N_b}\right).$$

3. Laboratory Investigation

Whereas the analysis of the circuit was made considering only square wave excitation, due to the relative ease of computing the firing angle (saturation time) with such excitation, both sinusoidal and square wave excitation were used in the laboratory in the investigation. In order to reduce unknown variations, the diodes and cores were matched as nearly as possible, although some core mismatch was still in evidence.

The primary concern was to determine if a minimum output significantly less than the static magnetizing current could be obtained by the use of AC bias. This point was chosen because it is the mimimum that can be obtained with DC bias. In practice the minimum obtainable is usually 50% to 100% greater than this value. The core used was orthonal, 1 mil - Magnetics Inc. #50425-1A, a 50% nickel iron alloy square loop material.

3.1 Sinusoidal Excitation

A minimum output of about one fourth of the minimum obtainable with DC bias was obtained with the use of both an AC and DC bias. This point was reached by adjusting the AC bias voltage to a minimum output. At this point the modal sequence changes as outlined in the circuit analysis. That the sequence changed at this point was confirmed in the laboratory by observing the core voltage on the oscilloscope. It was evident that the core was saturating in the resetting mode. Accompanying this modal sequence change was a blocking of the output diode

in the gating circuit and an unblocking of the diode associated with the resetting core. The analysis indicates the diode blocking and unblocking follows from the modal sequence change.

With the AC bias adjusted for minimum output an additional DC winding used as a bias winding was employed to reduce the minimum output to the lowest attainable. This value was significantly less than that obtained by use of only a DC bias, being less than one fourth of that value. The minimum output obtained with the AC bias alone was well above the static magnetizing current and somewhat larger than the value obtained with DC bias only. Thus if minimum output is an important consideration, it is necessary to use two bias windings, one for AC and one for DC.

It was found that if the AC bias was adjusted above the value for minimum output the resultant gain characteristic curve showed a marked gain decrease and lowering of maximum output. Values of AC bias voltage below the value required for minimum output did not result in gain characteristic deterioriation or lowered maximum output but did result in higher minimums.

3.2 Square Wave Excitation

For square wave excitation the minimum output obtainable with AC bias alone was lower than that obtainable with DC bias only. An additional DC bias winding lowered the minimum obtainable but introduced a marked nonlinearity in the gain characteristic which was basically a linear, very low gain,

portion followed by the normal high gain linear portion. The low gain linear portion corresponds to the change of modal sequence pointed out in the analysis. The results for sinusoidal and square wave excitation are summarized in the following graphs, Figure 6 and Figure 7.

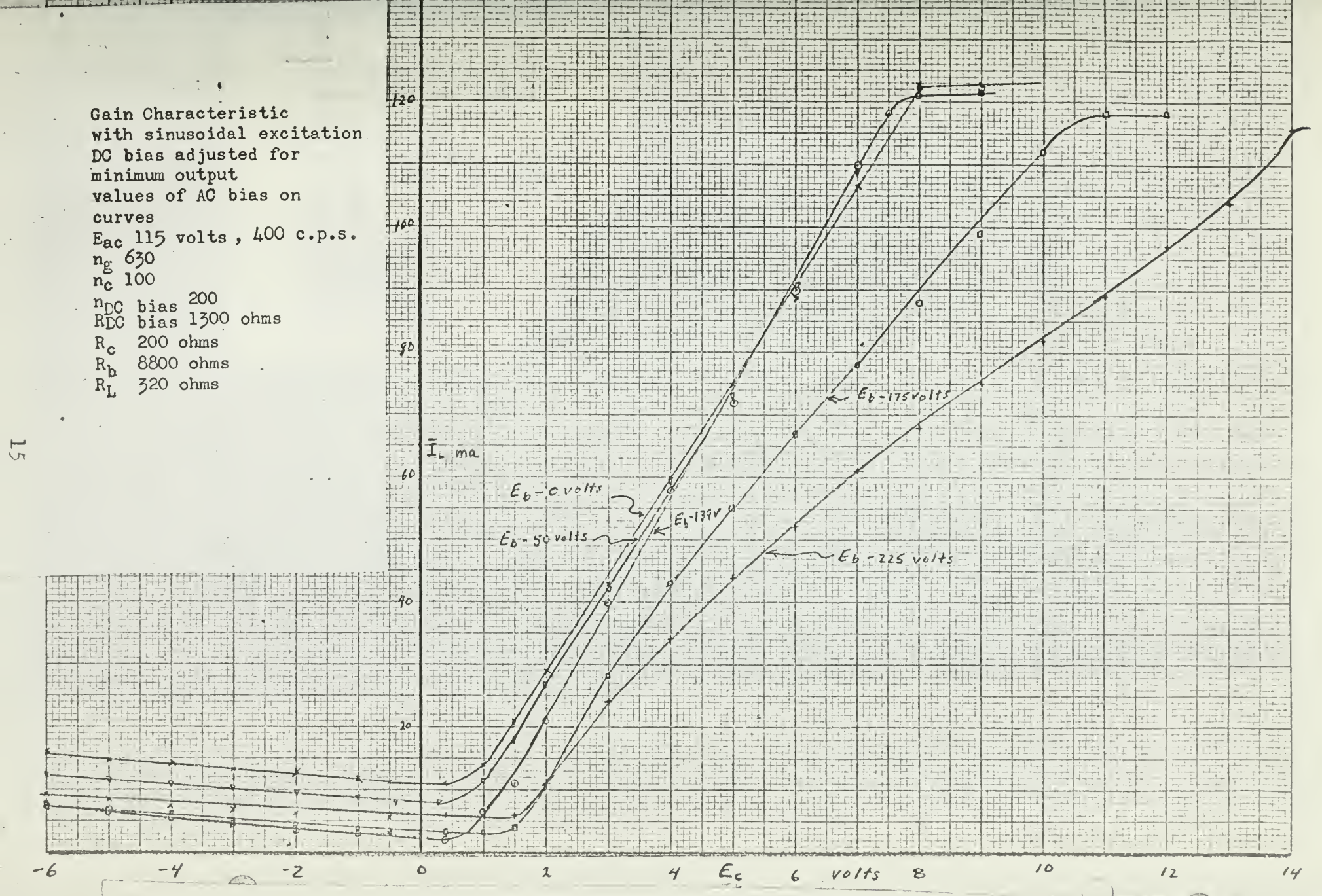


Fig. 6. Gain Characteristics with AC and DC bias sinusoidal excitation

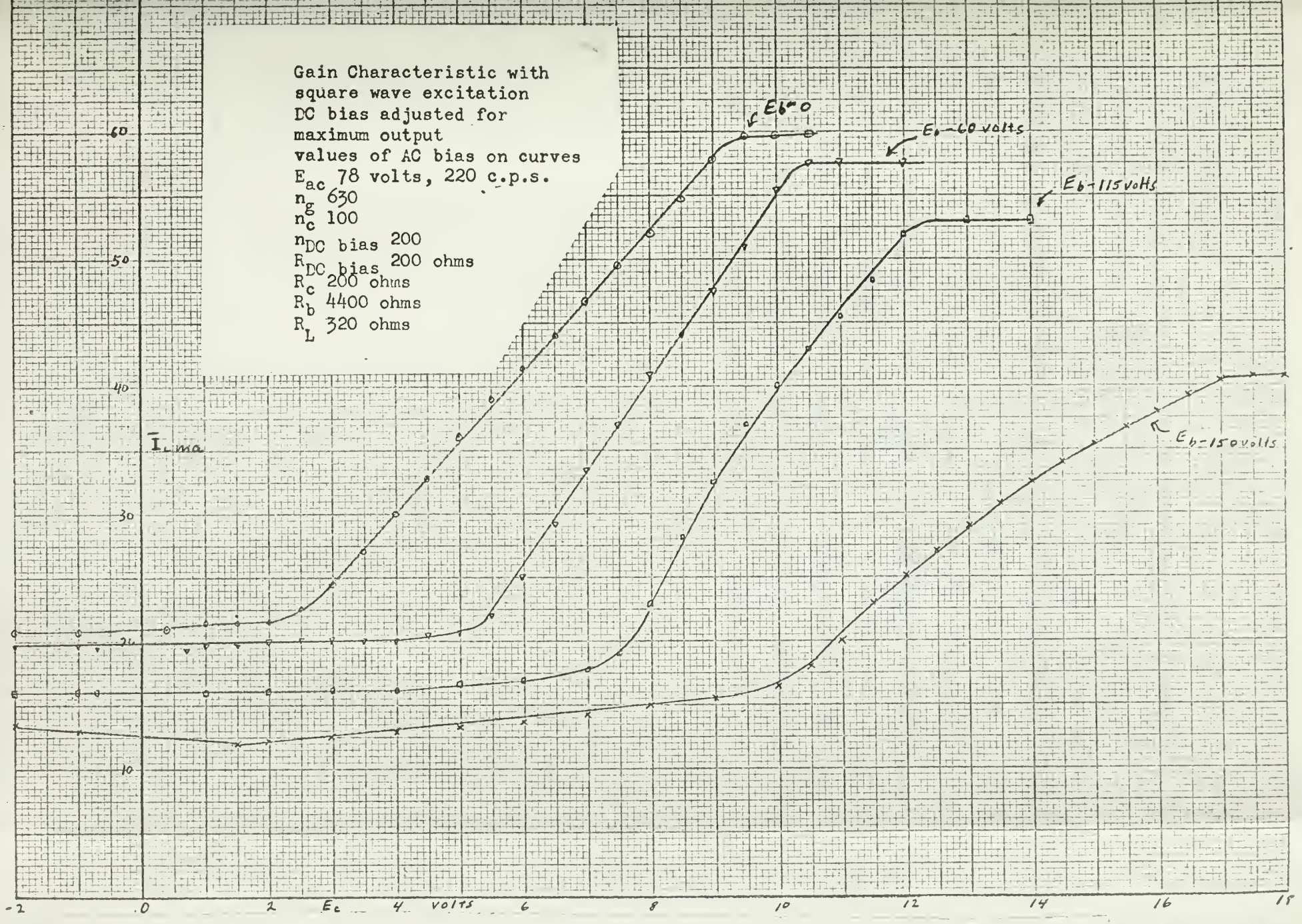


Fig. 7. Gain Characteristics with AC and DC bias square wave excitation

4. Conclusions

The use of an AC bias is very effective in reducing the minimum output for the center tap magnetic amplifier, particularly for a sinusoidal source voltage. This output however, is still not zero. As long as the AC bias voltage is not increased above that for minimum output with AC bias alone there is no deterioration in the gain characteristic slope or linearity. The results of the analysis can be interpreted in terms of AC control with DC bias or in terms of multiple inputs by replacing the single AC and DC terms by summations. For applications where minimum outputs are important two bias windings, AC and DC, are indicated.

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